Exhibit C

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MEDIATEK, INC. and MEDIATEK USA, INC.,
Petitioner,

v.

REDSTONE LOGICS LLC,
Patent Owner.

Case IPR2025-00085
Patent 8,549,339

PATENT OWNER'S PRELIMINARY RESPONSE

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I. Introduction

Neither of the Petition's two grounds addressing the independent claims demonstrates a reasonable likelihood of prevailing on demonstrating invalidity of any claim of the '339 Patent.

Both these grounds suffer the same flaw. Neither primary reference discloses a first and second PLL. Instead, MediaTek manufactures components that neither reference discloses. While both grounds cite the same secondary reference, neither ground articulates a basis for any combination with that reference for the PLL or clock signal limitations.

Likewise, both grounds also fail to identify a "first clock signal" that is "independent from the second clock signal" or a "second clock signal" at all. Instead, the petition vaguely references "independent operation" as sufficient. It is not. Where the petition identifies a first and second clock signal, they manufactured from whole cloth with no justification.

Accordingly, institution should be denied.

II. Background

A. MediaTek's Petition

Petitioner MediaTek, Inc. ("Petitioner" or "MediaTek") challenges claims 1-6, 8–11, 14, and 21 of U.S. Patent No. 8,549,339 (the "'233 Patent"). Petitioner structures its two asserted grounds for unpatentability as follows:

- Ground 1: Obviousness of claims 1, 5, 8–10, 14, and 21 over Knoth in view of Allarey
- Ground 2: Obviousness of claims 2–4 over Knoth and Allarey in view of Flautner.
- Ground 3: Obviousness of claim 6 over Knoth and Allarey in view of Wolfe and further in view of Kumar.
- Ground 4: Obviousness of claim 11 over Knoth and Allarey in view of Wolfe.
- Ground 5: Obviousness of claims 1–3, 5, 8–10, 14, 21 over Naffziger and Allarey.
- Ground 6: Obviousness of claim 4 over Naffziger and Allarey in view of Flautner.
- Ground 7: Obviousness of claim 6 over Naffziger and Allarey in view of Wolfe in further in view of Kumar.
- Ground 8: Obviousness of claim 11 over Naffziger and Allarey in view of Wolfe.

Because all challenged dependent claims across all grounds depend from claim 1, this Preliminary Response need only address the Petition's arguments concerning claims 1 and 21. If the Petition does not show a reasonable likelihood of prevailing on claims 1 and 21, then it cannot prevail on any other challenged claim.

B. Overview of the '339 Patent

At a high level, the '339 Patent is directed generally to a novel operation of a multi-core processor enabling coordination of groups of multiple cores operating at different supply voltages and clock signals. *See* Ex. 1001 at 2:4–3:15.

The '339 Patent explains: a "multi-core processor **[]** may be divided into stripes… [where e]ach stripe may be associated with an independent power profile … and/or may be associated with an independent clock domain defined by a clock signal received from a clock control block." *Id*. at 2:25–31. However, "[t]o maintain the limited differential relationship discussed above, adjusting the supply voltage to one stripe may involve adjusting the supply voltages to the other stripes." *Id*. at 3:8–10.

To address this, the '339 Patent describes an architecture to achieve this wherein "the stripe [] may be powered by a supply voltage received from a power control block[] and/or may be associated with an independent clock domain defined by a clock signal received from a clock control block[]." *Id*. at 2:26–31.

This solution to the prior art problem of dynamic management of sets of processor cores is reflected, for example, in claim 1 of the '339 Patent, which recites:

> 1. A multi-core processor, comprising:
> a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first output clock signal of a first phase lock loop (PLL) having a first clock signal as input;
> a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input,

> wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal; and
>
> an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.
>
> Ex. 1001 at claim 1.

All other challenged dependent claims 2-6, 8-11, and 14 depend from claim 1 and claim 21 reads similarly to claim 1.

III. Level of Ordinary Skill in the Art

The Petition proposes that a person of ordinary skill in the art in the field of the '339 Patent "would have had at least a bachelor's degree in electrical engineering, computer engineering, computer science, or a similar field, and at least two years of industry or academic experience designing or analyzing electronic circuits, semiconductors, processors, or power management, and related firmware and software, or the equivalent." Paper 1 at 6–7. For purposes of this preliminary response, Patent Owner does not challenge that definition.

IV. Claim Construction

The Petition states "the claim terms in the '339 Patent are accorded their ordinary and customary meaning that they would have to a person having ordinary

skill in the art at the time of the alleged invention." Paper 1 at 6. For purposes of this preliminary response, Patent Owner agrees.

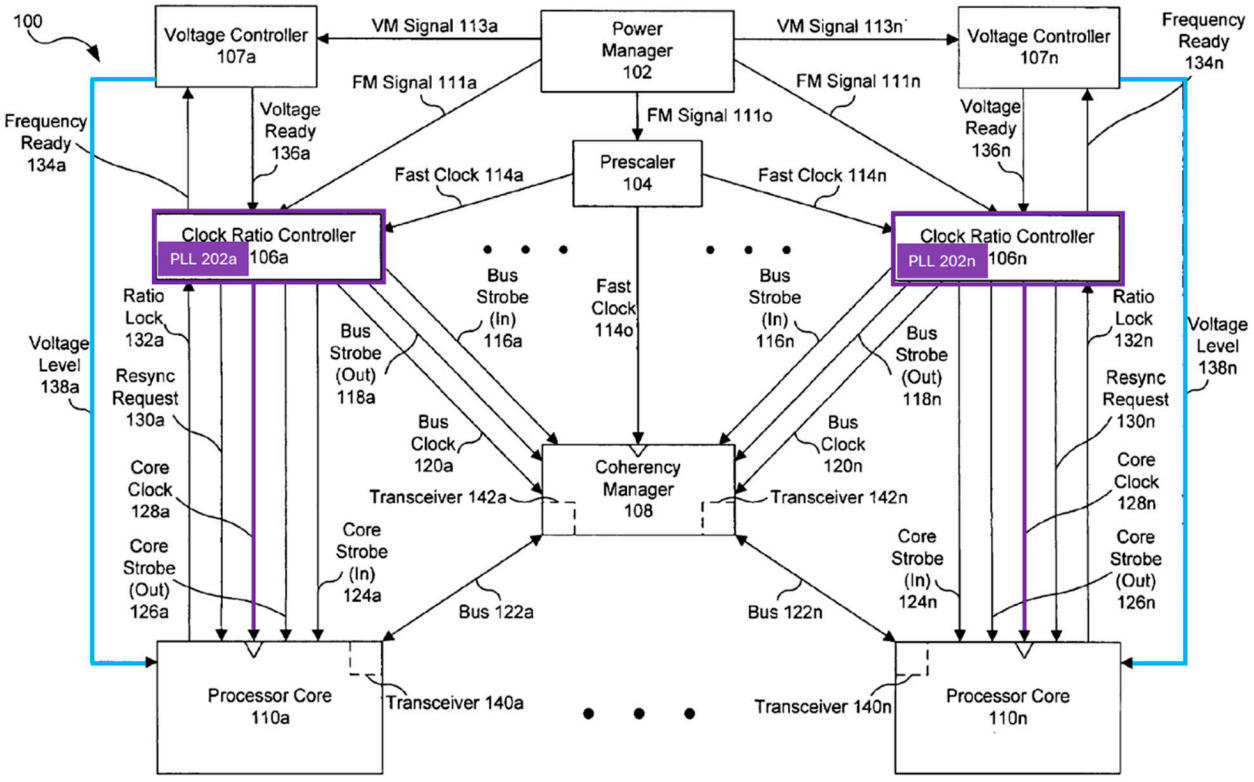
V. The Petition's Ground 1 Fails to Disclose The Claimed First and Second Clock Signals

The Petition fails to identify the key components claimed to enable the management of sets of, rather than individual, cores. Namely, the petition fails to identify a first and second PLL that respectively receive a first and second clock signals that are independent of one another. Instead, the Petition relies on Dr. Baker to manufacture these PLLs and associated clock signals with no explanation for why such would be obvious, inherent, or otherwise disclosed. Likewise, the Petition offers no explanation for why the manufactured clock signals would be independent of the clock signal that was actually disclosed. For any and all of these reasons, Ground 1 fails to demonstrate how any claim is obvious.

A. A First and Second PLLs Are Not Disclosed In the Art

Both challenged independent claims require a first and second PLL with respective first and second clock signals as inputs where the first clock signal is independent from the second clock signal. *See* Ex. 1001 at Cl. 1, 21. Mediatek's petition proposes a first and second PLL and accompanying first and second clock signals as inputs that are not disclosed in either Knoth or Allarey and not justified as obvious or inherent.

The Petition proposes that the claimed first and second PLLs can be found in either Knoth or Allarey but Knoth fails to disclose two PLLs and the Petition fails to justify any combination with Allarey. For Knoth, the Petition identifies PLL 202_a and PLL 202_n as a component of Clock Ratio Controller 106_a and 106_n. Paper 1 at 22-23.



Id. at 22. However, Knoth never discloses a PLL 202_a or PLL 202_n or any PLL that is a component of a Clock Ratio Controller 106. Both are an ex post invention of Dr. Baker. What Knoth actually discloses is the "clock ratio controller 106 is *coupled to* a phase-lock loop (PLL) 202 and prescaler 104 of digital system 100." Ex. 1005 at

[0041][1]. Indeed, the only figure that depicts any PLL, Figure 2A expressly excludes it from the Clock Ratio Controller 106 via a demarcating dotted line:

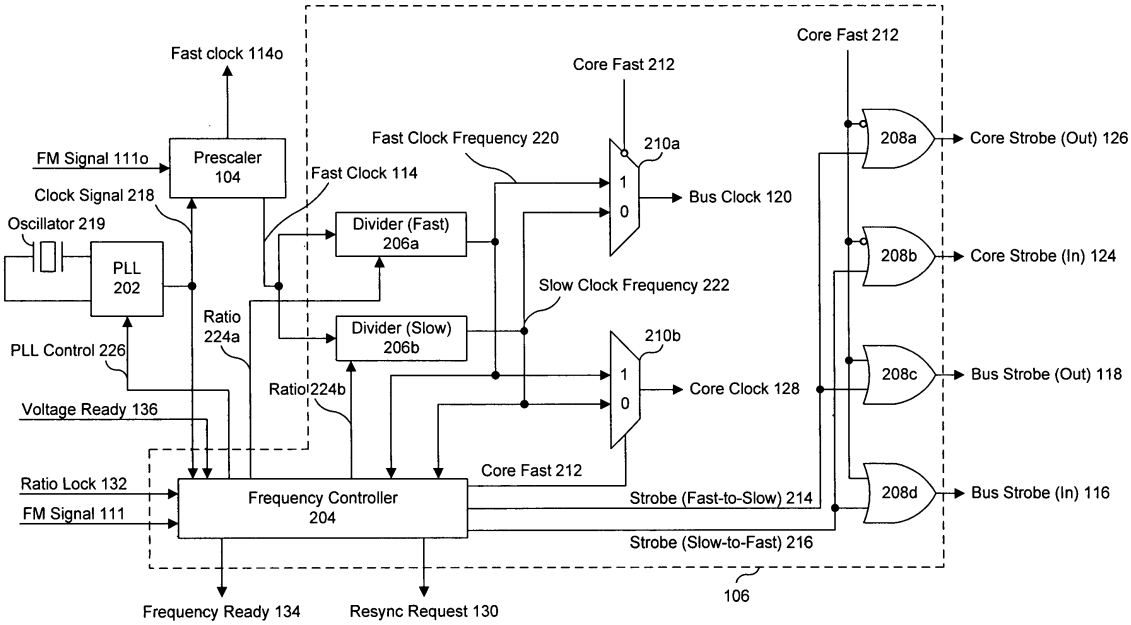


FIG. 2A

Id. at Fig. 2A.

The Petition has no explanation for its creation of an entire series of PLLs. Likewise, looking to Dr. Baker's declaration, there is nothing. At best, Dr. Baker suggests Fig. 2A "shows a representative clock ratio controller 106 that includes PLL 202 and an oscillator 219 [and a]s a result, clock ratio controllers $106_{a\text{-}n}$ each includes a phase locked loop (PLL) 202…" Ex. 1003 at ¶ 111. But, as noted above,

[1] All emphasis is added unless otherwise noted.

PLL 202 is expressly *not* part of the clock ratio controller 106. *See* Ex. 1005 at Fig. 2A and [0041]. Rather, the PLL 202 is treated much more like prescaler 104, a separate part of the digital system 100. *Id*. at [0041] ("clock ratio controller 106 is *coupled to* a phase-lock loop (PLL) 202 and prescaler 104 of digital system 100.") While Knoth discloses "a *plurality* of clock ratio controllers [and] a *plurality* of voltage controllers [and] a *plurality* of processor cores" all designated a–n, it only discloses a single prescaler 104 and a single PLL 202 and never similarly designates them. *Id*. at [0022]; [0041]. Because, as seen in Fig. 1 and discussion throughout Knoth, there is only one prescaler 104, the logical conclusion is that there is only one similarly disposed phase-lock loop 202. But even without making that logical determination, the Board should still reject Dr. Baker's leap as it has no basis or explanation under either obviousness or inherency. *See* 37 CFR § 42.65 ("Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.").

First, the petition simply makes no obviousness assertion as to this limitation within Knoth.[2] Second, a party suggesting inherency "must show that *the natural result flowing* from the operation as taught would result in the performance of the questioned function." *PersonalWeb Techs., LLC v. Apple, Inc.*, 917 F.3d 1376, 1382

[2] The Petition's reference to Allarey is addressed below.

(Fed. Cir. 2019) (emphasis original; internal citations and quotations omitted). Here neither the Petition nor Dr. Baker offer any such showing. Instead, as shown below in Naffziger single PLL systems were common and workable. *Infra* §VI.B.

The Petition's reliance on Allarey fares little better. While Allarey discloses two PLLs, there is no explanation for why or how Allarey's PLLs could be implemented into the teachings of Knoth, much less that a POSITA would. Indeed, all the Petition provides is a general motivation to combine and that "Allarey also discloses this limitation." Paper 1 at 16–18; 25. The Petition's general motivation to combine Knoth and Allarey has nothing to do with PLLs or why a POSITA would be motivated to use multiple as in Allarey where Knoth teaches only one. Instead, the general motivation to combine contends both references "relate to the same well-known technologies," "are directed to the same field of multi-core processors, address similar problems[,] and propose similar solutions for managing voltage and frequency scaling of multi-core processors." *Id*. at 16. But none of these explanations address what features would be taken from what reference, much less why. The *only* basis the Petition offers for a specific combination of Knoth and Allarey is that "a PHOSITA would have been motivated to modify Knoth to have two sets of cores, rather than two individual cores." *Id*. at 20. But this has no connection to the PLLs

of Allarey. Because there is no explanation for why Allarey's two PLLs would or could be implemented into Knoth, MediaTek has not shown it would be obvious.[3]

Indeed, the control system, including its use and placement of PLLs, seems counter to that taught in Knoth. Knoth suggests a centralized control system where a single "power management unit 102 provide individual frequency management (FM) signals [] to clock ratio controllers [] and individual voltage management (VM) signals." Ex. 1005 at [0025]. These signals initiate frequency and voltage adjustments individually for each core. *Id*. In contrast, Allarey teaches a decentralized system where "[e]ach site includes a phase locked loop (PLL) clock signal generation circuit, … each PLL can change the frequency of the clock signal through a relocking process." Ex. 1006 at 2:50–55. Allarey explains "each site with processor 100 might actively modify the frequency of the cores … [and] may need to modify the frequency of the clock signal being supplied to the cores by PLL 116 and PLL 118." It is unclear then why a system designed around a central power management unit dictating the voltage and frequency provided to the cores would implement the arrangement of a system designed for the cores to alter their own frequency.

[3] To be clear, Dr. Baker likewise presents no explanation of such a combination in his declaration. Indeed, the discussed sections are largely parroted from Dr. Baker's declaration where he provides nothing more.

As the Petition offers no additional analysis for claim 21 and instead merely cites back to sections of claim 1 discussed above, *see* Paper 1 at 49–51, these criticisms apply equally to claim 1 and 21.

B. First and Second Clock Signals as Input Are Not Disclosed In the Art

The Petition's failure to identify a first and second PLL compounds when the "having a first/second clock signal as input" limitation is considered. Without the claimed second PLL, as in Knoth, there can be no second clock signal as input and Allarey discloses no clock signals as input at all.

For Knoth, the Petition suggests two options for the first and second clock signals, "the timing pulses from oscillator 219_a[4], or alternatively, PLL control signal 226_a," Paper 1 at 24, both fail. While the first option, the timing pulses, is a clock signal, there is only one such signal not a first and second signal as claimed. As with PLL 202, Knoth only discloses a single Oscillator 219 providing only a single timing pulse. Ex. 1005 at [0042]. The single oscillator is depicted as outside of any clock ratio controller 106 (*Id*. at Fig. 2A) and MediaTek identifies no basis for multiplying either an oscillator or a timing pulse to each clock ratio controller. A single signal cannot satisfy either the need for a first and second clock signal.

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[4] Again, there is no 219_a disclosed in Knoth, only a 219 that is separate from any clock ratio controller 106. *See* Ex. 1005 at [0041].

MediaTek's alternative, PLL control signals, are simply not clock signals. Knoth explains "clock ratio controller 106 includes frequency controller 204" and "PLL 202 is controlled by frequency controller 204 using a PLL control signal 226." Ex. 1005 at [0042], [0044]. But neither MediaTek nor Dr. Baker explain why a frequency controller's PLL control signal would be considered a "clock signal" by a POSITA. This is particularly jarring when Knoth itself uses the term "clock signal" with regards to a variety of other signals. *See e.g. id*. at [0042] ("PLL 202 outputs a clock signal 218"); [0043] ("prescaler 104 provides clock signal 218 to clock ratio controller 106 as a fast clock signal 114"). The '339 Patent explains a "clock signal" drives the processor core. Ex. 1001 at 4:4–10. This is the same as Knoth explains its "clock signals" but not PLL control signal. *Compare* Ex. 1005 at [0044] ("Core fast signal 212 is used to indicate whether an associated processor core 110 is to be driven by the output of clock signal divider 206_a or the output of clock signal divider 206_b.") *with* [0061] ("Programmable logic array 250 may also control PLL 202 using PLL control signal 226."). A "clock signal" and a "control signal" are clearly different signals and a PLL control signal does not meet the first and second clock signal limitation. Further, as noted above, Knoth only discloses a single PLL, thus even if a PLL control signal were a "clock signal," Knoth does not disclose "a second PLL having a second clock signal as input."

Allarey does not even disclose inputs to its PLLs and neither Dr. Baker nor MediaTek contend otherwise. *See* Ex. 1003 at ¶ 121 ("Allarey discloses that the first set of cores (cores in site 0) dynamically receives a first supply voltage and a first output clock signal of a first PLL (PLL for site 0)."). Rather, Allarey only teaches "[e]ach PLL is capable of generating a clock signal that the cores located at each respective site can use as a reference clock." Ex. 1006 at 2:52-54. Even if the PLLs of Allarey could or would have been combined with any teaching of Knoth (and MediaTek has not shown such), there would be no first and second clock signals as inputs.

C. The First Clock Signal is Independent from the Second Clock Signals as Input Is Not Disclosed In the Art

All these failures come to a head at the "first clock signal is independent from the second clock signal" limitation. In order to meet this limitation, the Petition relies on only one proposed modification: incorporating a second oscillator. The Petition contends a "PHOSITA would read Knoth to include independent first and second PLLs within clock ratio controllers 106_a and 106_n, respectively, receiving the first and second clock signals (the timing pulses generated by oscillators 219_a and 219_n) that are independent from each other." Paper 1 at 28-29. While the Petition cites Dr. Baker's declaration, he only provides the exact same conclusory language. *See* Ex. 1003 at ¶¶ 131-32.

As explained above, Knoth discloses only a single PLL, a single oscillator, and instance of timing pulses. Neither the Petition nor Dr. Baker's declaration explain why it would be obvious or inherent or would be a PHOSTIA's reading that multiple PLLs, oscillators, or sets of timing pulses could or would be used. And even if the Board accepts that multiple PLLs would be used, that does not disclose multiple independent clock signals as claimed, much less the specific modification relied on in the Petition where the multiple independent clock signals correspond to multiple oscillators.

Indeed, this is the express teaching of Naffziger discussed below. *Infra* §VI.B. Such a device would not have a first and second clock signal, just one clock signal sent to two locations. And even if the Board were to accept multiple oscillators, despite neither Knoth or Allarey teaching such, the Petition offers no explanation for why they would be "independent from each other" as posited by MediaTek. Because the alternative, PLL control signals, are not clock signals, they likewise cannot disclose this limitation.

MediaTek's discussion of Allarey also fails. All MediaTek can contend is that "the first PLL clock signal generation circuit is independent from the second PLL clock generation circuit." Paper 1 at 29. But that is not what is claimed. The claims are not concerned with whether the PLLs, or their associated circuits, are independent, but rather if the input clock signals are. *See* Cl. 1, 21. Even if

MediaTek's conclusion on the independence of Allarey's circuits was supported, it is not, it is entirely irrelevant. Allarey does not disclose "the first clock signal is independent from the second clock signal."

Ground 1 of the Petition fails to demonstrate the claimed first and second PLLs having a respective first and second clock signal as input or the first clock signal is independent from the second clock signal are obvious. First, the Petition does not demonstrate Knoth discloses a first and second PLL or that it would be obvious to incorporate the first and second PLLs from Allarey. Second, Knoth fails to disclose a second clock signal as input and Allarey does not disclose any clock signals as inputs. Last, because neither Knoth nor Allarey disclose a first and second clock signal, neither discloses or renders obvious "the first clock signal is independent from the second clock signal." As such, Ground 1 does not demonstrate any of the challenged claims are obvious much less establish a reasonable likelihood of prevailing at a Final Written Decision.

VI. The Petition's Ground 5 fails for the Same Reason.

Ground 5 suffers the same flaw as Ground 1. There is no disclosure in Naffziger of a second PLL. Instead, Dr. Baker simply invents one. This creation deletes the mode expressly taught by Naffzigger with no explanation offered in the Petition for why Naffzigger's teachings would be disregarding or why a second PLL would be used instead. Likewise, the Petition offers no basis for incorporating any

teaching of Allarey with regard to PLLs or clock signals. As such, just as above, Ground 5 fails to demonstrate the claimed first and second PLLs having a respective first and second clock signal as input or that the first clock signal is independent from the second clock signal are obvious.

A. Ground 5 Discloses Only One PLL

The challenged claims all require a first and second PLL. MediaTek provides only a single theory for Naffziger disclosing two PLLs, that "[a] PHOSITA reading Naffziger would have understood that the multi-core processor 500 includes more than one power control unit 150 each associated with a corresponding core[,]" thus providing a "first power control unit 150A" and a "second power control unit 150B" each contain a PPL. Paper 1 at 69. But Naffziger does not teach multiple power control units instead, it expressly teaches using only a single power control unit.

Naffziger expressly teaches "[p]ower control unit 150 is configured to monitor the power of *both* processor cores 105A and 105B…" Ex. 1010 at [0053] (emphasis added). Indeed, Figure 5 shows only a single power control unit 150 is used and provides "clk_core_1" and "clk_core_2" to Cores 1 and 2:

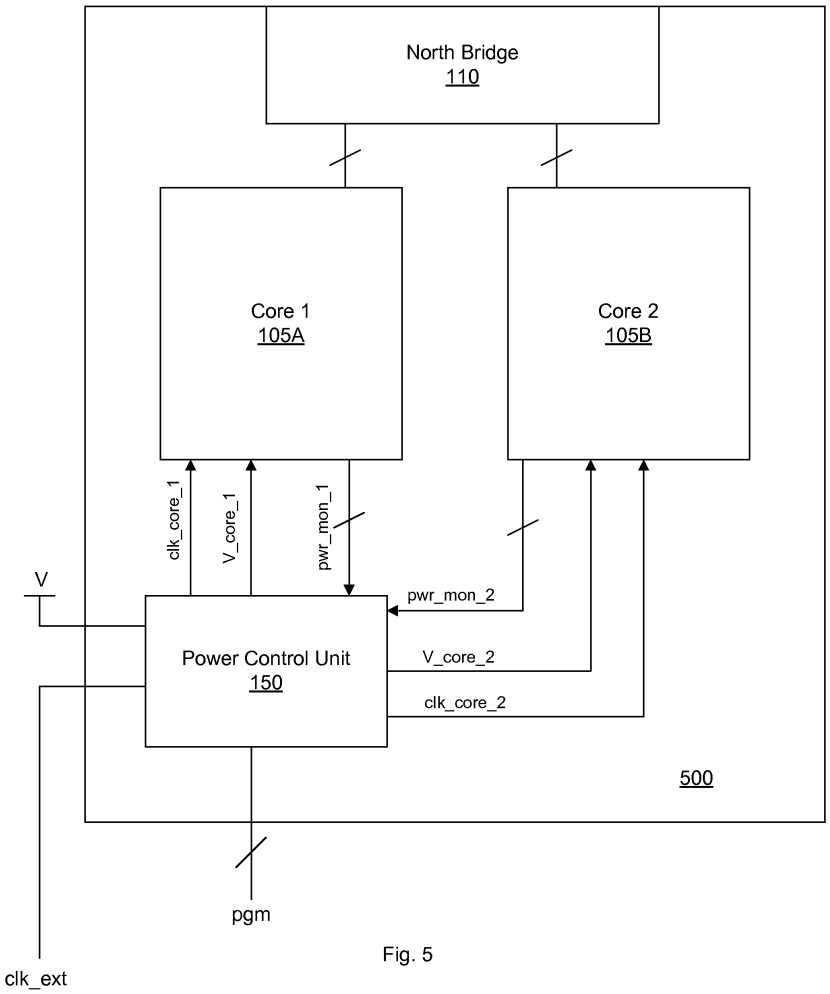
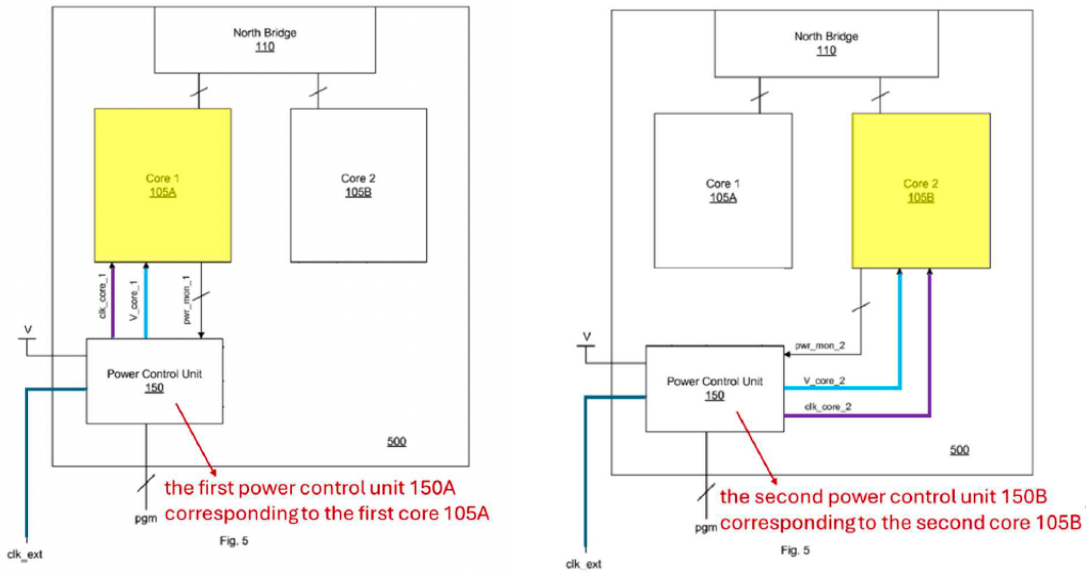


Fig. 5

Compared with Dr. Baker's "annotated" figures he simply cuts out the inconvenient connects without support in Naffziger or explanation for why a POSITA might do so:



Ex. 1003 at ¶¶ 248, 257. Even where Naffziger contemplates "processor cores 105A and 105B may be controlled independently of one another" only one power control unit is used. *See* Ex. 1010 at [0054]. Naffziger teaches "power control unit 150 is configured to monitor the processing workloads of each processor core 105A and 105B, and may change operational states of the cores by changing their *respective* processing workloads." *Id*. (Emphasis added).

The Petition does not allege the addition of power control units would be an *obvious* implementation of Naffziger. *See* Paper 1 at 68–70 (providing no motivation to modify Naffziger to satisfy this limitation); *see also* Ex. 1003 at ¶250 (alleging "[a] PHOSITA reading Naffziger" would understand there is a power control unit for each core); ¶¶ 248–254 (alleging no obviousness ground for this limitation except to note "Allarey also discloses this claim limitation.")

To the extent MediaTek wishes to pursue an inherency argument, it has no support. Again, to show inherency "a party must show that *the natural result flowing* from the operation as taught would result in the performance of the questioned function." *PersonalWeb Techs., LLC v. Apple, Inc.*, 917 F.3d 1376, 1382 (Fed. Cir. 2019) (emphasis original; internal citations and quotations omitted); *see also PAR Pharm., Inc. v. TWI Pharms., Inc.*, 773 F.3d 1186, 1196 (Fed. Cir. 2014) ("in order to rely on inherency … the limitation at issue necessarily must be present, or the natural result of the combination of elements explicitly disclosed by the prior art"). MediaTek offers nothing more than the conclusion that a PHOSITA would understand multiple power control units from Naffziger's teaching of 1. *See* Paper 1 at 69. Dr. Baker is no better offering the exact same statement. *Compare id*. with Ex. 1003 at ¶ 250. As shown above, Naffziger expressly teaches a single power control unit, it cannot be that it is "the natural result flowing from the operation" of a single power control unit to use two. Without any contrary evidence, MediaTek has not shown Naffziger expressly or inherently discloses a second PLL.

This leaves Allarey. As noted above, Allarey discloses two PLLs but just as in Ground 1, MediaTek provides no obviousness argument as to Allarey's PLLs. Instead, Ground 5 merely notes "Allarey also discloses this limitation." Paper 1 at 71, 73; *see also* Ex. 1003 at 254 (noting the same). Again, the only specific basis MediaTek provides for combining anything from Allarey into Naffziger is to

combine the sets of cores taught by Allarey into Naffziger. *See* Paper 1 at 67–68. But this has nothing to do with the PLLs and does not show that they could or would be combined into the teaching of Naffziger. All the Petition provides then is generalized reasons to combine Naffziger and Allarey. These reasons, ranging from both Naffziger and Allarey being directed to multi-core processors and being authored by engineers at peer companies (Paper at 65–67) fail to explain why or how a PHOSITA would have taken Allarey's PLLs and combined them into Naffziger's processor. At best, Dr. Baker identifies that "Allarey studies stabilizing a supplied voltage during a clock signal frequency locking process" and a PHOSITA might want this feature in Naffziger. Ex. 1003 at ¶ 238. But Dr. Baker never ties this feature of Allarey to the PLLs. As such there is no basis to suggest the Petition offers an obviousness argument for this limitation.

B. Ground 5 Discloses Only One Clock Signal as Input and Does Not Show Any Clock Signal is "Independent"

MediaTek contends "[a] PHOSITA would read Naffziger to include independent first and second power control units receiving the first and second clock signals that are independent from each other." Paper 1 at 74–75. But MediaTek never explains how a PHOSITA conclude 1) Naffziger discloses a first and second power control units or 2) the clock signals they receive as inputs would be independent from each other. A PHOSITA would not reach these conclusions.

Patent Owner has addressed the first above. The second fares no better. Naffziger teaches only a single "clk_ext" which MediaTek identifies as both the first and second clock signals, Paper 1 at 69, 72. Naffziger explains the "power control unit is coupled to receive an external clock signal, clk_ext, from a source external to processor 100." Ex. 1010 at [0022]. As shown in Figure 5 this signal is provided to the single power control unit which in turns provides separate clock signals to both cores:

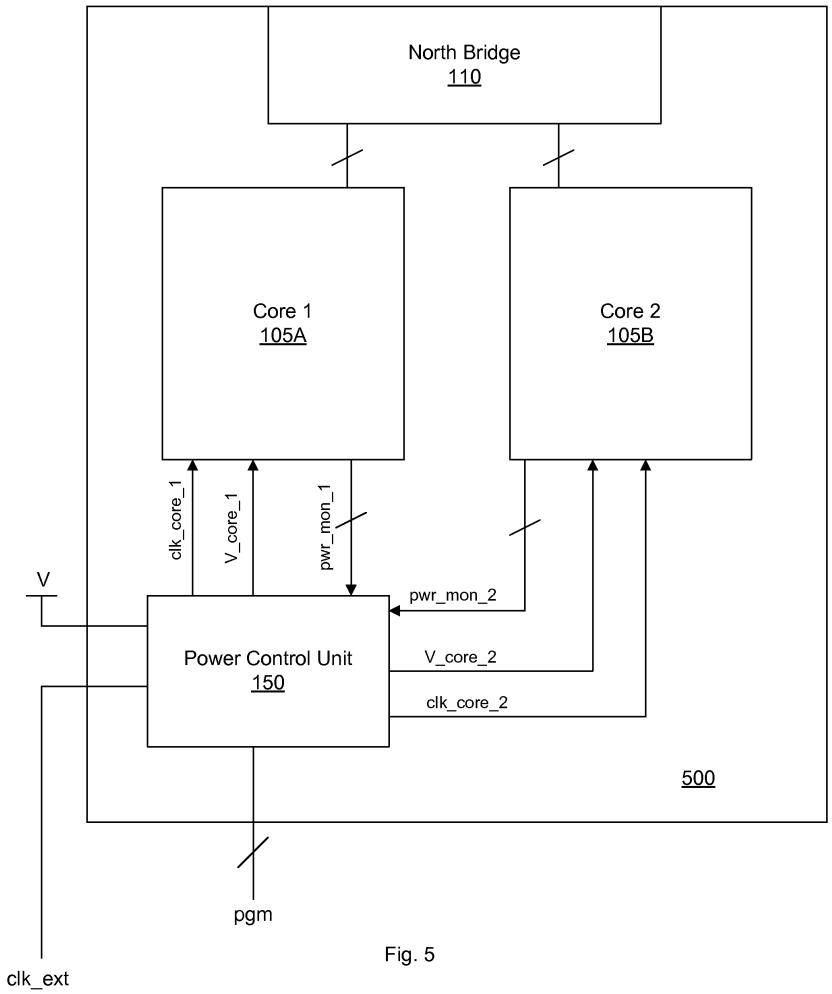


Fig. 5

Id. at Fig. 5. The express teaching of Naffziger is a single external clock signal supplied to a single Power Control Unit and then processed to provide clock signals to the cores.

In light of this evidence, MediaTek can only parrot a single paragraph from Dr. Baker:

> Naffziger discloses this limitation. Ex[1003], ¶ 264. As discussed for Claim 1[a2] and [b2]-[b3] in Ground 5, Naffziger discloses that the multi-core processor system includes separate, independent power control units associated with the cores—for example, the first power control unit 150A corresponding to the first core 105A and the second power control unit 150B corresponding to the second core 105B—and each power control unit receives as an input an external clock signal. A PHOSITA would read Naffziger to include independent first and second power control units receiving the first and second clock signals that are independent from each other. *Id*.

Paper 1 at 74-75; *see also* Ex. 1003 at ¶ 264 (same). But this offers no basis to suggest a PHOSITA would have found it obvious or inherent to 1) duplicate the power control unit and 2) supply the duplicated power control unit with a separate, independent external clock signal. It provides no motivation for the alteration and, as discussed above, is counter, not a natural result of, the express teaching of Naffziger.

While MediaTek contends Allarey also discloses "the first clock signal is independent from the second clock signal," it does not. As noted above, Allarey does not teach any clock signals as inputs to its PLLs. MediaTek recognizes this in its Ground 1, cited in Ground 5, only alleging the PLL circuits are independent, not any clock signal is. Further, neither MediaTek nor Dr. Baker provide any basis for combining anything from Allarey with Naffziger for this limitation.

Ground 5 does not show a second PLL, a second clock signal as input to that PLL, or that the first clock signal as input is independent from any second clock

signal. Instead, Naffziger teaches only a single PLL with only a single input and MediaTek provides no basis for adding a second PLL let alone a second clock signal as input that is independent of the first. Likewise, while Allarey discloses two PLLs it does not disclose any input clock signals and MediaTek provides no basis to combine Allarey with Naffziger for these limitations. Accordingly, the Petition cannot show invalidity of either claim 1 or claim 21 on the basis of Ground 5.

VII. Denial of Institution under *Fintiv* is Warranted.

35 U.S.C. § 314(a) gives the Board discretion to deny institution of IPR due to the advanced state of parallel district court litigation regarding the same issues. *See NHK Spring Co. v. Intri-Plex Techs., Inc*., IPR2018-00752, Paper 8 at 19-21 (PTAB Sept. 12, 2018) (precedential) ("*NHK*"). The Board has set forth six factors for determining whether discretionary denial in light of such parallel litigation is appropriate, and in analyzing them, "takes a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review." *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 5–6 (PTAB Mar. 20, 2020) (precedential) ("*Fintiv I*"); *see also Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 15 at 7-17 (PTAB May 13, 2020) (informative) ("*Fintiv II*"); Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation (dated June 21, 2022) ("Interim Discretionary Denial Memo," Ex. 1060).

Each of these six *Fintiv* factors weigh in favor of the Board exercising its discretion to deny institution here. For Factor 1, no stay of the parallel district court litigation has been granted or requested, and a stay is unlikely given the advanced stage of the case. For Factor 2, the district court trial will occur within weeks of the deadline for a final written decision in this proceeding. For Factor 3, largely due to Petitioners' delay in filing the Petition, there will be much investment by the parties and the district court—by the time the Board issues its institution decision, the *Markman* hearing will have occurred, and final infringement and invalidity contentions will be served. For Factor 4, there is substantial overlap in both the patent claims and art at issue in this proceeding and in the district court, and Petitioner failure to file its promised stipulation does not quell the concerns of inefficiency and inconsistent rulings. For Factor 5, Petitioner is a defendant in the parallel litigation. And for Factor 6, not only did Petitioners unduly delay in filing the Petition, but the Petition fails to present a compelling challenge on the merits and its supporting expert is unreliable. Each of these factors is addressed in more detail below.

A. *Fintiv* Factor 1: The district court has not granted a stay, nor is there any evidence that a stay will be granted.

In the parallel district court proceeding involving the same claims of the '339 patent, the district court has not granted a stay pending IPR. Further, Petitioner has

not requested such a stay, there is no indication it will do so, and there is no evidence that a stay will be granted.

Moreover, the facts here indicate that it is unlikely that the district court would grant a stay pending IPR even if this IPR were instituted, given the late stage of litigation. The parties have already exchanged infringement contentions, invalidity contentions, and claim construction disclosures. Ex. 1015. And by the time the Board's institution decision is due in this proceeding (April 22, 2025), the Court will have conducted the *Markman* hearing and a claim construction order will have issued or will soon issue, final infringement and invalidity contentions will be served and fact discovery will close in five months. *See* Ex. 1015. Further, trial is currently set for May 4, 2026, two weeks after the earliest deadline for a final written decision in this IPR. *Id.*; *see infra* § VII.B.

Thus, even if Petitioner were to file a motion for a stay pending this proceeding, it is highly unlikely a stay would be granted at this late juncture in the case.

Where the district court litigation has not been stayed, and any stay is speculative and unlikely, allowing this IPR to proceed in parallel would be wasteful and inefficient. Factor 1 weighs against institution.

B. *Fintiv* Factor 2: The district court trial will occur within weeks of the deadline for a final written decision in this proceeding.

"If the court's trial date is earlier than the projected statutory deadline, the Board generally has weighed this fact in favor of exercising authority to deny institution under *NHK*." *Fintiv I* at 9.

Here, the deadline for a final written decision in this IPR is April 22, 2026, which may be extended to October 22, 2026, for good cause or in the case of joinder. 37 C.F.R. § 42.100(c). Meanwhile, the district court litigation is set for trial on May 4, 2026. *See* Ex. 1015.

Because the district court trial is currently set to occur within weeks of the earliest deadline for a final written decision in this IPR this factor is fairly neutral.

C. *Fintiv* Factor 3: By the time an institution decision is reached, the Court will have held the *Markman* hearing and final contentions will be served.

Factor 3 relates to the "amount and type of work already completed in the parallel litigation by the court and the parties ***at the time of the institution decision***." *Fintiv I* at 9. For example, "if, at the time of the institution decision, the district court has issued substantive orders related to the patent at issue in the petition," this factor favors denial. *Id.* at 9-10. "Likewise, district court claim construction orders may indicate that the court and parties have invested sufficient time in the parallel proceeding to favor denial." *Id.* at 10.

Here, by the time the institution decision issues, the *Markman* hearing will be

complete and a *Markman* order will have issued or will soon issue. The *Markman* decision would clearly qualify as a "substantive order." But even if the *Markman* order does not issue prior to the institution decision, in any event, claim construction proceedings will be complete, and the district judge would have taken these substantive issues under submission. Ex. 1015. Final contentions will likewise have been served. *Id.*

These investments by the parties and district court weigh against institution because they ensure that this IPR cannot be an efficient alternative to district court litigation. This favors discretionary denial, and panels have found this factor to favor denial when the parallel litigation was at a similarly advanced stage as here. *See, e.g.*, *BOE Tech. Grp. Co. v. Element Capital Commercial Co.*, IPR2023-00808, Paper 9 at 23-24 (PTAB Nov. 15, 2023) (denying institution in part because claim construction was complete); *Roku, Inc. v. IOEngine, LLC*, IPR2022-01551, Paper 11 at 12 (PTAB May 5, 2023) (same); *10X Genomics, Inc. v. President & Fellows of Harvard College*, IPR2023-01299, Paper 15 at 18 (PTAB Mar. 7, 2024) (same); *Samsung Elecs. Co. v. Mojo Mobility Inc.*, IPR2023-01094, Paper 11 at 9 (PTAB Feb. 9, 2024) (same).

Of course, the reason that the district court litigation will be so far along at the time of institution is because Petitioners unduly delayed in filing the Petition, filing over eight months after service of the district court complaint. *Compare* Pet. at 102

(dated October 22, 2024) *with* Ex. 2001 at 1 (Petitioner was served on January 30, 2024). The Petition offers no explanation for Petitioner's delay.

Because there has been substantial investment in the parallel proceeding, and Petitioners delayed in filing the Petition, Factor 3 weighs heavily against institution.

D. *Fintiv* Factor 4: There is substantial overlap between this IPR and the district court proceeding.

This factor looks at "whether all or some of the claims challenged in the petition are also at issue in district court" and whether the "petition includes the same or substantially the same claims, grounds, arguments, and evidence" as the parallel district court case. *Fintiv I* at 12–13. Here, the challenged and asserted claims are identical, and the prior art relied upon in the Petition and at the district court is substantially overlapping.

First, the Petition challenges claims 1–6, 8–11, 14, and 21 of the '339 patent; those are also the same claims currently asserted in the litigation. *Compare* Pet. at 3 (challenging claims 1–6, 8–11, 14, and 21) *with* Ex. 2002 at 2 (infringement contentions asserting claims 1, 5, 8–10, 14, and 21); *see also Pharaoh Energy Servs., LLC v. Flex-Chem Holding Co.*, IPR2024-00815, Paper 7 at 13–14 (PTAB Sept. 20, 2024) (denying institution in part because the same claims were challenged at the PTAB and asserted in litigation); *Vector Flow* at 22 (same); *EClinicalWorks* at 12 (same).

Further, Petitioner's promised stipulation to "not pursue in the parallel litigation any ground that is raised or that could have reasonably been raised in an IPR," does not address efficiency concerns rooted in that substantial overlap. Petitioner has not filed such a stipulation and thus is only questionably bound by its representation.

In short, the Petition challenges the same patent claims that are asserted in the parallel litigation, and Petitioner promised stipulation is yet to materialize. This raises substantial "concerns of inefficiency and the possibility of conflicting decisions," weighing against institution. *See Fintiv I* at 12.

E. *Fintiv* Factor 5: Petitioner is a defendant in the district court litigation.

Petitioner is a defendant in the parallel litigation. *See, e.g.*, *Fintiv II* at 15 ("Because the petitioner and the defendant in the parallel proceeding are the same party, this factor weighs in favor of discretionary denial.").

F. *Fintiv* Factor 6: Other circumstances weigh strongly against institution, including the weakness of the Petition and Petitioner's delay.

This factor looks at "other circumstances that impact the Board's exercise of discretion, including the merits." *Fintiv I* at 9. This factor weighs heavily against institution for two reasons.

First, contrary to Petitioner's assertion, the merits of this Petition suffer from significant weaknesses and gaps in proof, as discussed above. *See supra* §§ V, VI.

Second, there is evidence that the Petitioner unduly delayed in filing the Petition, doing so less than four months before the statutory deadline, and the Petitioner offers no explanation for the delay. *See supra* § VII.C.

* * *

Each of the six *Fintiv* factors supports the Board exercising its discretion to deny institution.

VIII. Conclusion

For the reasons set forth above, Patent Owner respectfully requests that the Board deny institution of the Petition. Both Grounds 1 and 5 rely on an unsupported addition to the prior art that a second PLL and second clock signal would exist and that the second clock signal would be independent of the first clock signal. But the Petition never shows these additions would be obvious or inherent.

Date: February 5, 2025

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CERTIFICATION REGARDING WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), Patent Owner certifies that there are 6,452 words in the paper excluding the portions exempted under 37 C.F.R. §42.24(a)(1).

Date: February 5, 2025

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CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e)(1))

The undersigned hereby certifies that the above document was served on February 5, 2025, by filing this document through the Patent Trial and Appeal Board Cast Tracking System as well as delivering a copy via electronic mail upon the following attorneys of record for the Petitioner:

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